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| L22 | L19 and l4 | 29 | L22 |
| L21 | L19 and l3 | 109 | L21 |
| L20 | L19 and l11 | 16 | L20 |
| L19 | (wait$4 or delay$4) near4 buffer$1 near15 (schedul$5 or issu$6 or fetch$6 or dispatch$6 or prefetch$6) | 578 | L19 |
| L18 | l12 and l7 | 9 | L18 |
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| L16 | l12 and l3 | 45 | L16 |
| L15 | l12 and superscalar | 37 | L15 |
| L14 | l11 and (wait$4 or delay$4) near4 buffer$1 | 34 | L14 |

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|---|---|---|---|
| L13 | L12 and (wait$4 or delay$4) near4 buffer$1 | 0 | L13 |
| L12 | L11 and dependen$6 near5 (matrix or mtrices) | 46 | L12 |
| L11 | (cam or content near3 addressable) and renam$5 near5 register$1 | 302 | L11 |
| L10 | l2 and l7 | 15 | L10 |
| L9 | l2 and l6 | 14 | L9 |
| L8 | l2 and l4 | 24 | L8 |
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| L6 | (711/123-221)![CCLS] | 17131 | L6 |
| L5 | (712/23)[CCLS] | 685 | L5 |
| L4 | (712/23)![CCLS] | 685 | L4 |
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| L2 | L1 and renam$5 near5 register$1 | 68 | L2 |
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